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IEEE JNL IEEE Journal or Magazine

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IEEE CNF IEEE Conference Proceeding

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IEEE STD IEEE Standard

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- ☐ 1. **Modeling non-slicing floorplans with binary trees**
Balasa, F.;
Computer Aided Design, 2000. ICCAD-2000. IEEE/ACM International Conference on
5-9 Nov. 2000 Page(s):13 - 16
Digital Object Identifier 10.1109/ICCAD.2000.896443
[AbstractPlus](#) | Full Text: [PDF\(472 KB\)](#) IEEE CNF
- ☐ 2. **On the exploration of the solution space in analog placement symmetry constraints**
Balasa, F.; Maruvada, S.C.; Krishnamoorthy, K.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE on
Volume 23, Issue 2, Feb. 2004 Page(s):177 - 191
Digital Object Identifier 10.1109/TCAD.2003.822132
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(1256 KB\)](#) IEEE JNL
- ☐ 3. **Efficient solution space exploration based on segment trees placement with symmetry constraints**
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- ☒ 4. **Placement with symmetry constraints for analog layout using trees**
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Digital Object Identifier 10.1109/ISCAS.2003.1206326
[AbstractPlus](#) | Full Text: [PDF\(391 KB\)](#) IEEE CNF

- ☐ **5. Using red-black interval trees in device-level analog placement symmetry constraints**
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21-24 Jan. 2003 Page(s):777 - 782
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- ☐ **6. A constraint-based placement refinement method for CMOS layout**
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Volume 6, 30 May-2 June 1999 Page(s):408 - 411 vol.6
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[AbstractPlus](#) | Full Text: [PDF\(348 KB\)](#) IEEE CNF

- ☐ **7. Device-level placement for analog layout: an opportunity for topological representations**
Balasa, F.;
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Digital Object Identifier 10.1109/ASPDAC.2001.913319
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- ☐ **8. Loop-closing and planarity in topological map-building**
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Volume 2, 28 Sept.-2 Oct. 2004 Page(s):1511 - 1517 vol.2
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- ☐ **9. Predicting conserved hairpin motifs in unaligned RNA sequences**
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Tools with Artificial Intelligence, 2003. Proceedings. 15th IEEE International Conference on
3-5 Nov. 2003 Page(s):10 - 17
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- ☐ **10. Block placement with symmetry constraints based on the orthogonal slicing representation**
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